17.3 A 3.4Mb/s RFID Front-end for Proximity Applications Based on a Delta-modulator

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Radio Frequency Identification (RFID) systems are used all over the world and cover a large spectrum of applications. The frequency bands used in such systems are at 125kHz, 13.56MHz or within the UHF ISM bands. Data rates range from some kb/s up to a few hundreds of kb/s. However, some emerging applications, such as national identity cards or multimedia, require larger data files to be downloaded and this implies higher data rates in order to maintain an acceptable transaction time. For this reason, the well-known ISO14443 13.56MHz standard [1] dedicated to personal identification extends the maximum data rate from 106kb/s to 847kb/s.

To increase the RFID communication data rate up to several Mb/s, without dramatically decreasing reading distance, a multilevel modulation scheme is proposed. A 4-level AM signal is proposed for Proximity Coupling Device (PCD – or reader) to Proximity Integrated Circuit Card (PICC – or card) communication. For PICC to PCD communication, a 4-phase load-modulation with a 1.7MHz sub-carrier is preferred. The circuit presented in this paper is a RFID front end, called EPSIS, which manages this high data-rate protocol by means of a delta-modulator architecture. The circuit can also be used at lower data rates, as it is compliant with the current ISO14443-B. The EPSIS delta-modulator has two functions: (1) create a regulated power supply, and (2) digitize the input signal into a bit stream which is later demodulated digitally. The circuit contains all required RFID analog functions (remote powering, voltage limitation and regulation, demodulation, back-scattering, clock recovery).

The overall circuit architecture is illustrated in Fig. 17.3.1. In 13.56MHz RFID systems, the reader and card coils are magnetically coupled [2]. Current flowing through the reader coil induces an electromagnetic force in the card coil that is amplified by the LC resonant circuit connected to EPSIS CoilA and CoilB inputs. The overall supply voltage for EPSIS, *Vdb,* is obtained at the output of the *Bridge* circuit which rectifies the voltage between CoilA and CoilB. An on-chip capacitance filters *Vdb*.

A voltage *Limiter* is connected to the coil inputs in order to: (1) protect circuit inputs against over-voltages which might occur when the card enters an RF field, and (2) increase the RF magnetic field dynamics for which the delta modulator loop works correctly.

The *References Generator* generates stable voltage references and bias currents for the circuit. The reset is managed by the *Power on Reset* block. The *Start of Frame* produces logical signals for data transfer synchronisation and threshold calibration. The *Carrier Clock Recovery* produces a 13.56MHz (F_0) digital clock whereas a 2×13.56MHz ($2F_0$) digital clock is produced in the *Clock Frequency Doubler*. F_0 is selected for low data rate communication and $2F_0$ for high data rate ones. *Retro-modulation* manages PICC to PCD communication: 2 NMOS transistors shunt current from the coil terminals to *gnd* to modify the LC circuit Q factor.

The heart of the EPSIS circuit is the delta-modulator illustrated in Fig. 17.3.2. The sampled *Delta-Modulator* loop controls the gate voltage (*Vcmd*) of two large shunt transistors. These transistors are connected to the coil inputs, controlling the Q factor of the LC resonant circuit.

To perform regulation and demodulation, the delta modulator uses a specific rectified voltage *RefPlim* (2V), produced by a *Coil Voltage Shaping block*. The *Voltage Shifter* is used to adapt *RefPlim* at the *Latch Comparator* positive input. Comparison between this shifted voltage and a *Reference Voltage* (0.9V) produces a 1b digital signal b_0 in synchronization with the *clock* signal (F_0 or $2F_0$). The *Charge-Pump* acts as a 1b DAC and integrator to produce the shunt voltage command *Vcmd*. The integrator consists of a 200pF capacitor charged or discharged by a 12µA current. When the regulation loop is closed thanks to shunt transistors a steady 1.8V *Vdb* voltage is obtained.

Figure 17.3.3 reports delta-modulator graphs obtained with an amplitude modulated stimuli (Graph 1) at a data rate of 1.7Mb/s. For a stabilized magnetic field, the b_0 signal oscillates periodically between its high and low values, which correspond to an alternate pumping up and down sequence of the *charge-pump*. The result is a stabilized *Vcmd* voltage (containing small oscillations due to charge pump sequence) applied to the shunt transistors gates. T_{b0s}, a main feature of the delta-modulator loop, is the period of b_0 when a constant magnetic field is applied. Magnetic field variations are counterbalanced by a *Vcmd* voltage variation to keep *Vdb* constant. For instance, if the magnetic field decreases, the *charge-pump* pumps down for a longer time than it does with a steady magnetic field in order to decrease *Vcmd*. Hence b_0 stays low for more than half of T_{b0s}. The reverse phenomena occurs if the magnetic field increases, with b_0 then staying high for more than half of T_{b0s}. In both cases, after *Vcmd* reaches the equilibrium point, b_0 recovers its periodic sequence with T_{b0s} period. The delay for which b_0 stays high or low before recovering its periodic sequence is proportional to the amplitude of the magnetic field variation. Graph 3 shows the b_0 response to input stimuli. By counting the number of sampling clock periods between two b_0 transitions, it is possible to quantify the magnetic field variations. Graph 4 is an example of a basic integration algorithm that sums up the 16 previous b_0 samples (+1 for b_0 high and –1 for b_0 low). An appropriate digital filter then retrieves the input data stream.

Bandwidth and stability of the loop must be optimised in order to reduce T_{b0s} duration and jitter, enabling the maximum data rate to be reached. Graphs 5 and 6 illustrate the main stability issues: a transient phenomena may appear before b_0 recovers its standard periodic sequence (period T_{b0s}). A low-pass FIR is applied to b_0 to eliminate this effect.

Figure 17.3.4 illustrates the PCD to PICC link measurement results in the 3.4Mb/s configuration. The magnetic field amplitude (Graph 1) is modulated by 4 predefined levels with a symbol time of 590ns ($8/F_0$). The sampling clock is $2F_0$, giving 16 b_0 samples per symbol (Graph 2). Graph 3 is the low pass FIR filter output.

The EPSIS chip is implemented in a 6M, 0.18µm, 1.8V, digital CMOS process from STMicroelectronics. The chip micrograph is shown in Fig. 17.3.5. The test chip area is 1.65×1.65mm² of which the main part is devoted to I/O (28 I/O for test purposes) or *Vdb* filtering capacitance. Active functions fit in 0.75mm², which can be reduced to less than 0.5mm² by removing analog test options. A full characterization has been performed at 1.7Mb/s with a BER better than 10^{-8}. At 3.4Mb/s a BER better than 10^{-6} is expected.

Acknowledgements:
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References:
[1] ISO/IEC 14443: Identification cards–Contactless integrated circuit(s) cards–Proximity cards, 2000.
[2] K. Finkenzeller, RFID Handbook: fundamentals and applications in contactless smart cards and identification, 2nd ed.,Wiley & Sons, 2003.

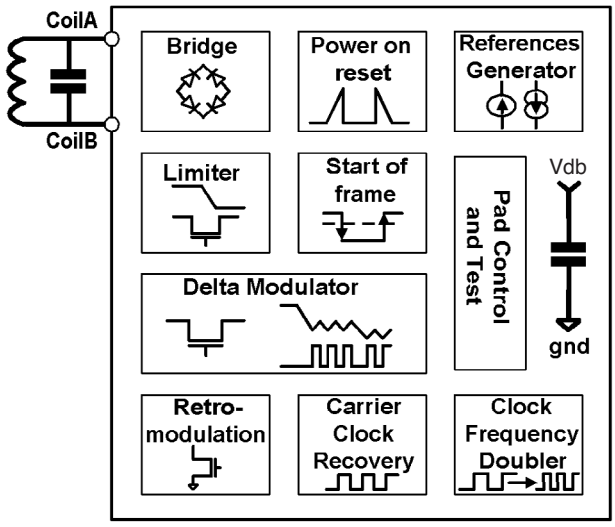

Figure 17.3.1: Front-end architecture.

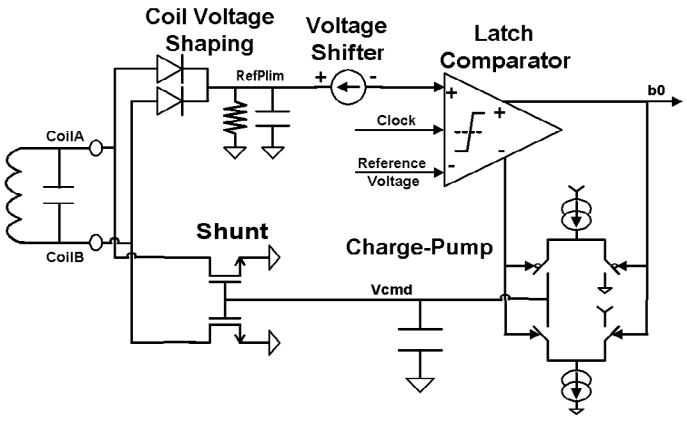

Figure 17.3.2: Delta modulator regulation and demodulation loop.

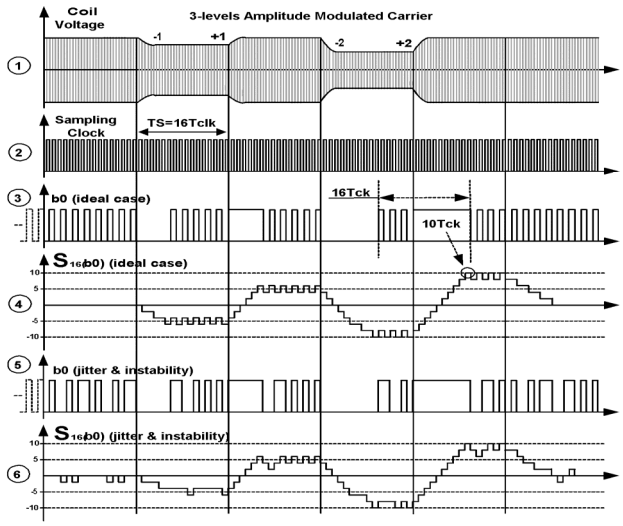

Figure 17.3.3: Circuit response to a multi-level AM stimuli.

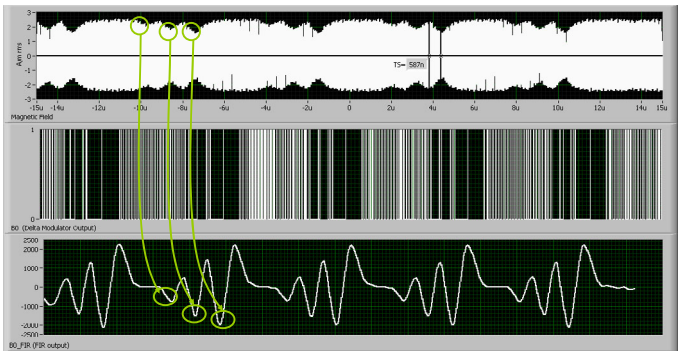

Figure 17.3.4: PCD to PICC link measurement at 3.4Mb/s.

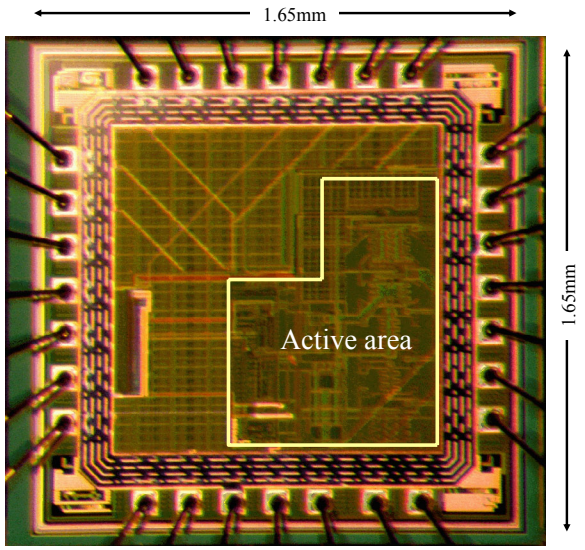

Figure 17.3.5: EPSIS chip micrograph.